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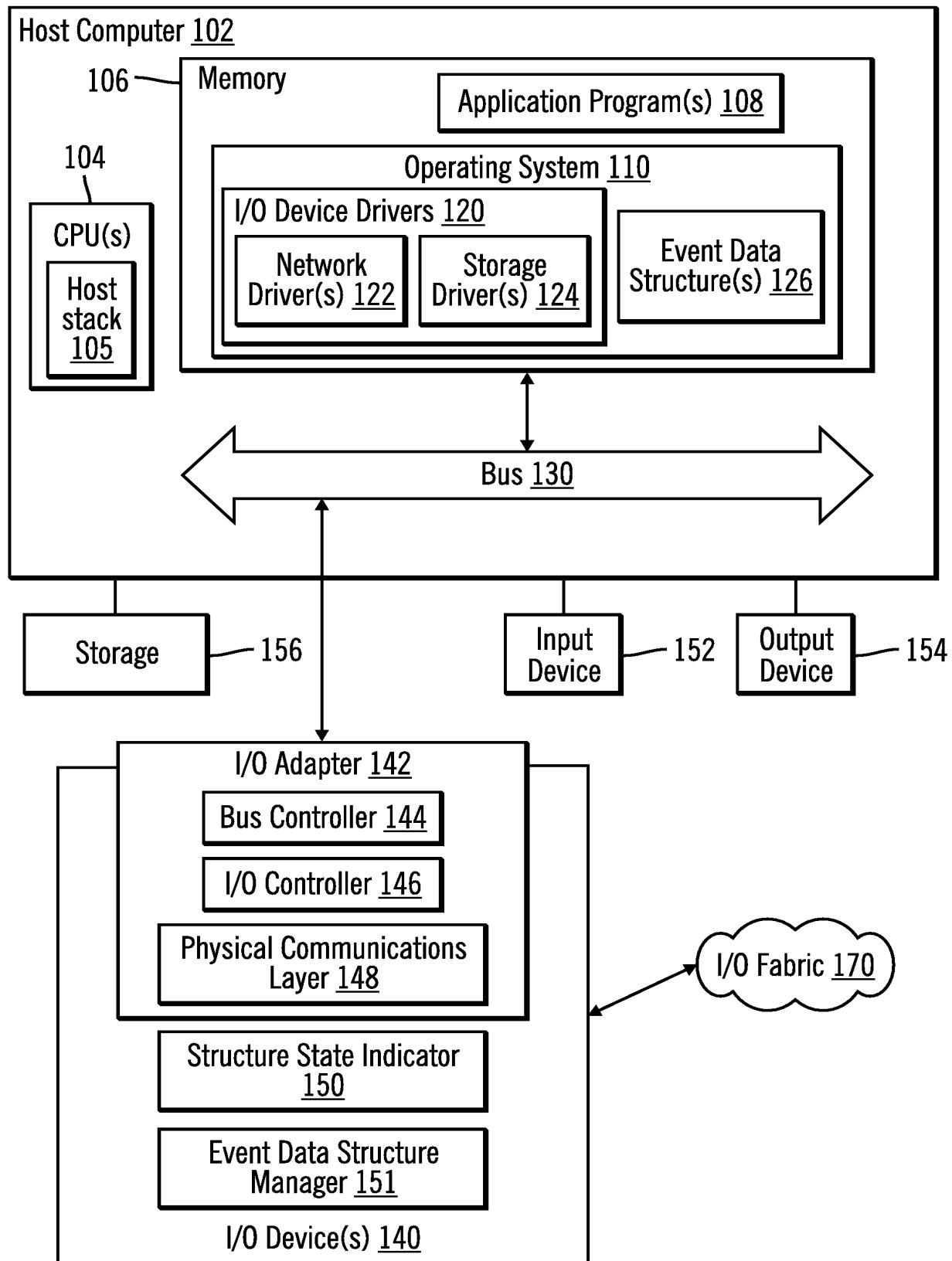


FIG. 1

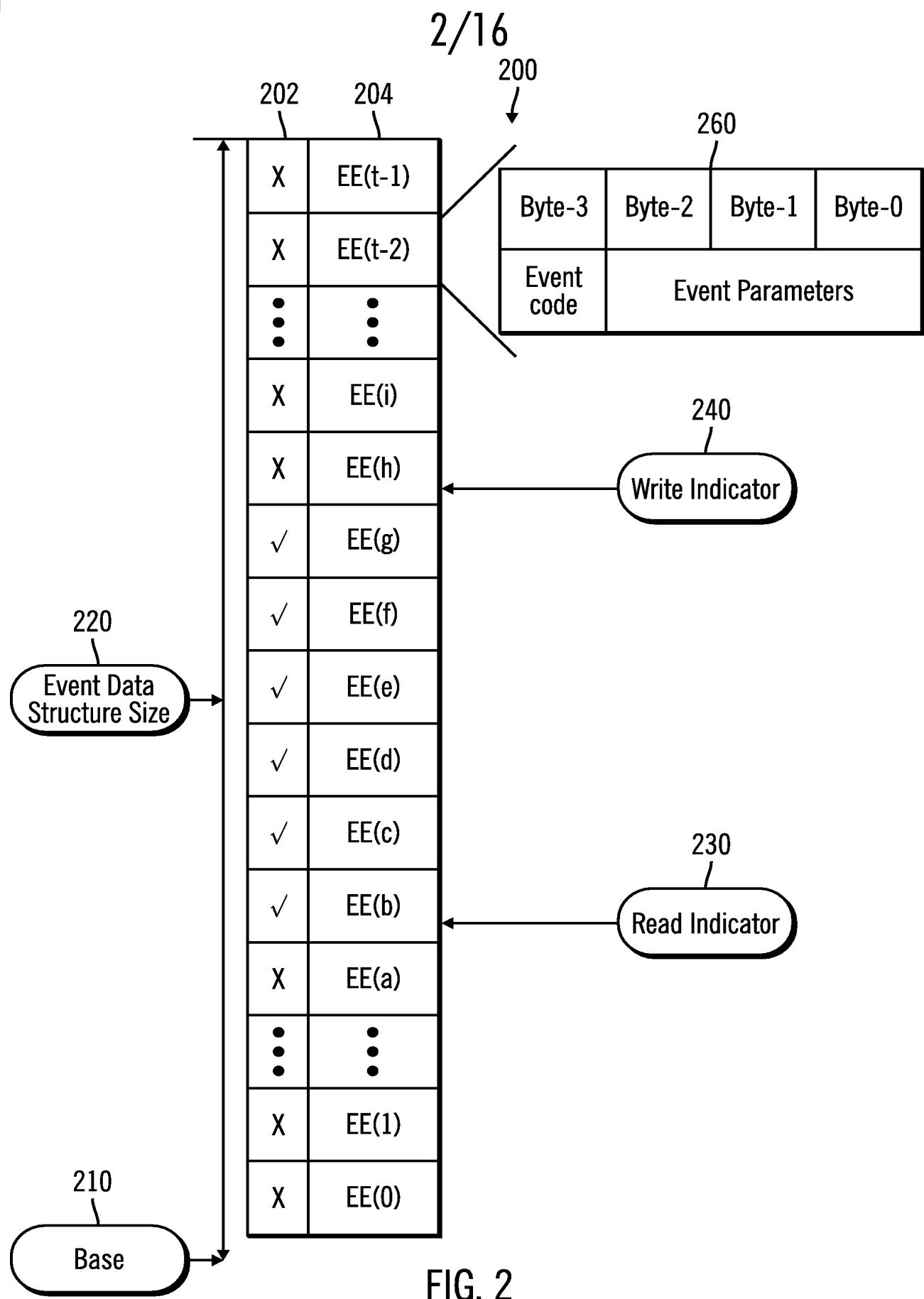


FIG. 2



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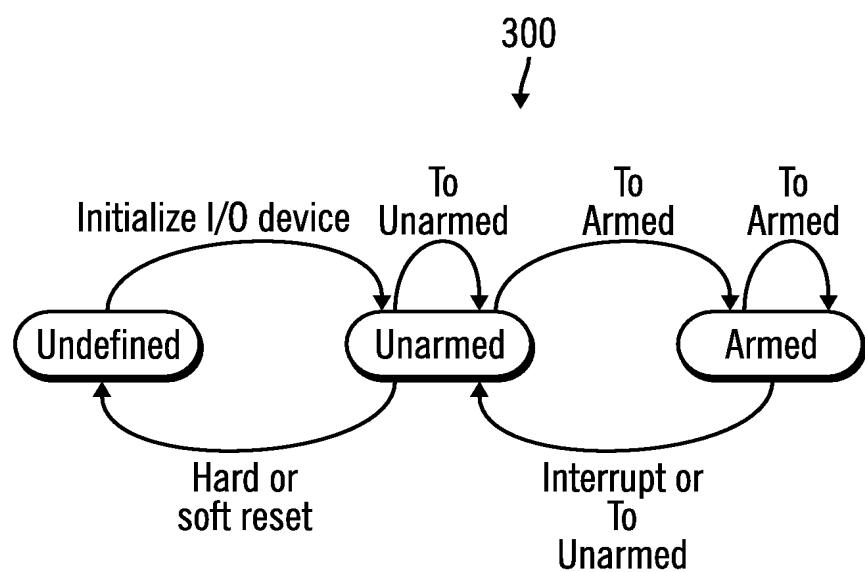


FIG. 3



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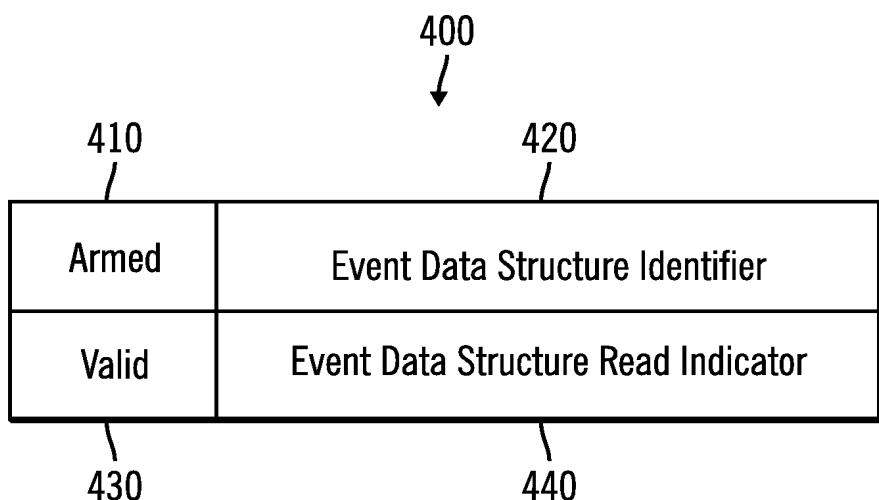


FIG. 4

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REPLACEMENT SHEET

INTERRUPT SCHEME FOR AN INPUT/OUTPUT DEVICE
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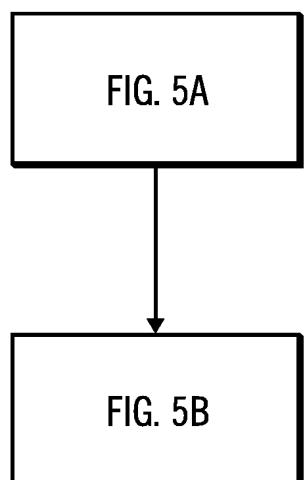


FIG. 5

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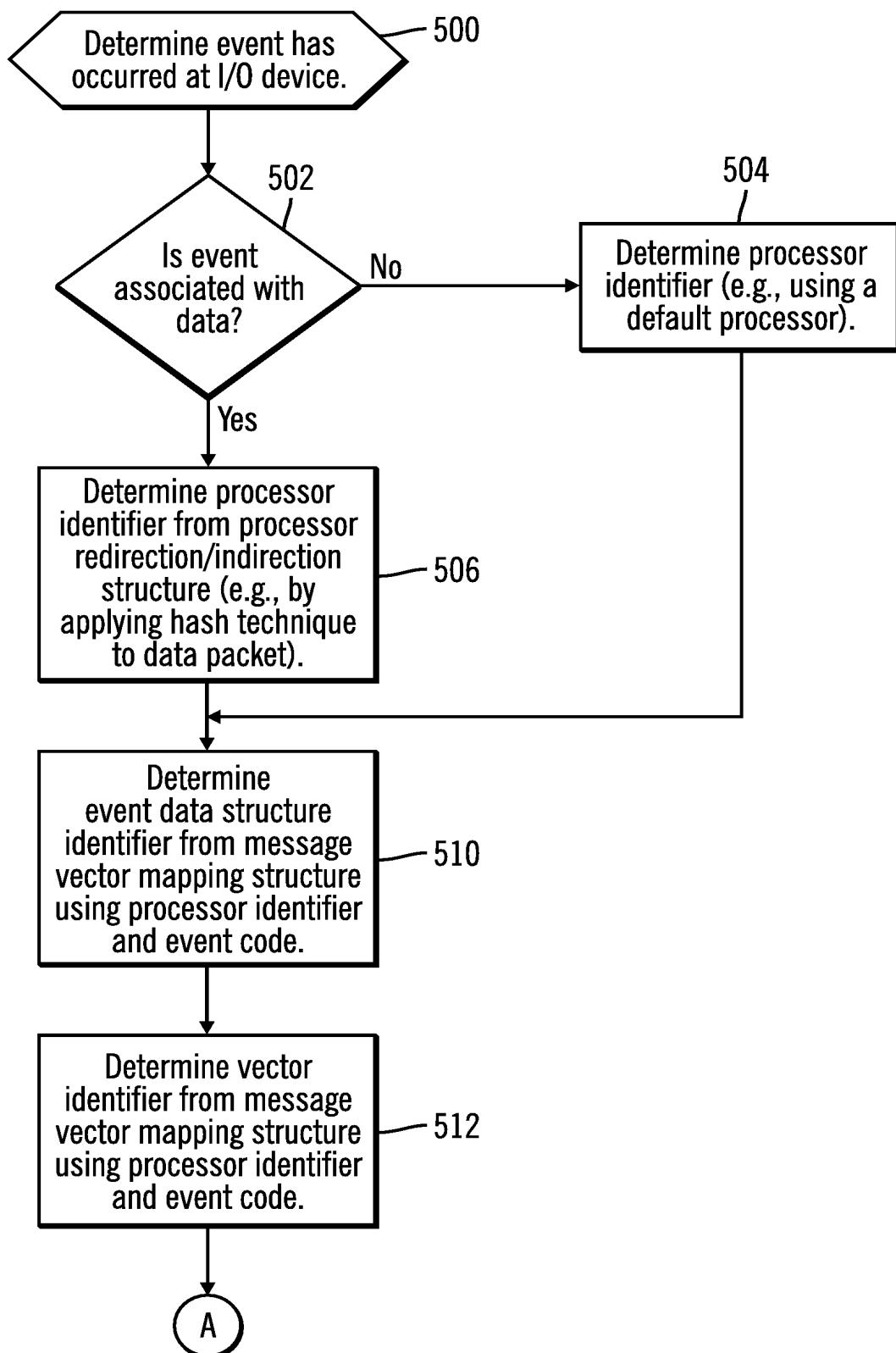


FIG. 5A

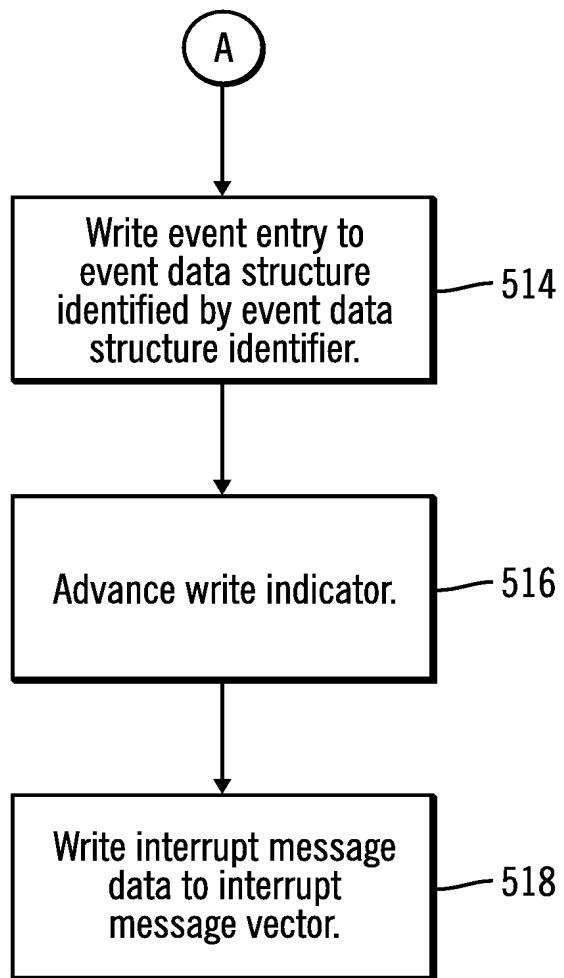


FIG. 5B



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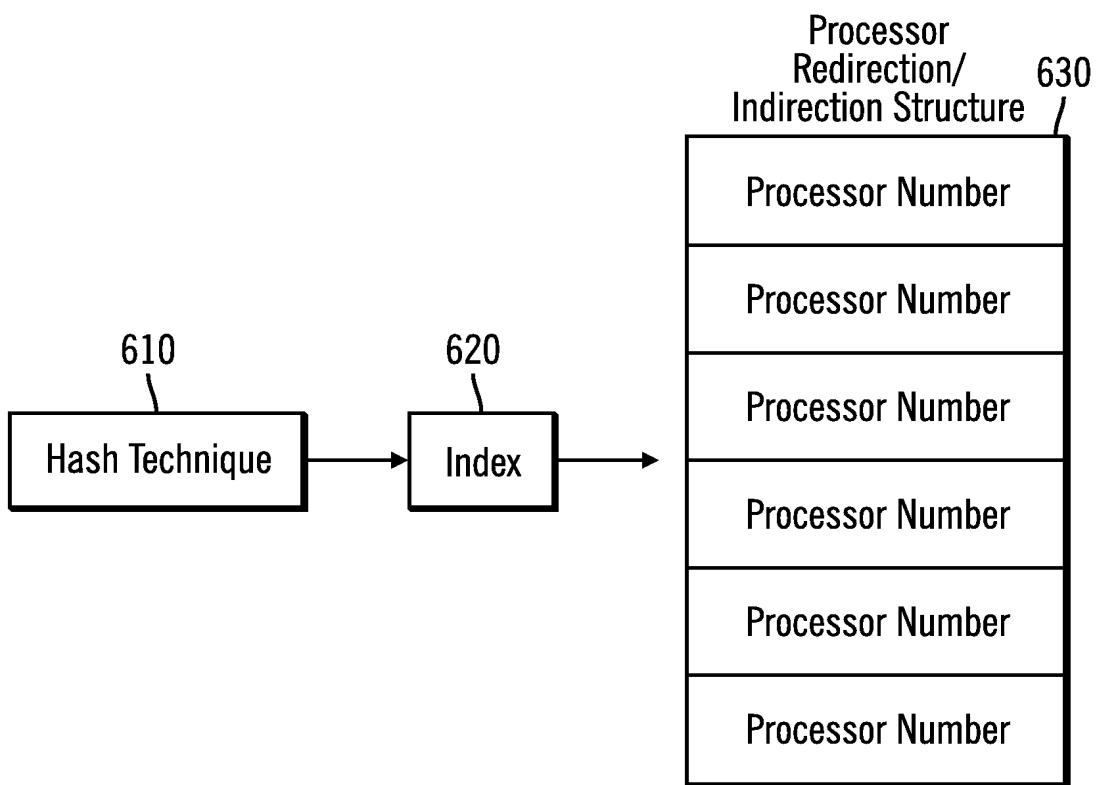


FIG. 6

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Message Vector Mapping Structure

Function/ Event Code	Processor 0	Processor 1	Processor 2	• • •	Processor N
RDMA	Event Data Structure Identifier	Vector Identifier			
Channel	• • •	• • •			
Global	• • •	• • •			
MGMT trap	• • •	• • •			

700

710 720

730 740

FIG. 7

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Message Vector Mapping Structure

Function/ Event Code	Processor 0	Processor 1	Processor 2	...	Processor N
RDMA TX	Event Data Structure Identifier	Vector Identifier			
RDMA RX	Event Data Structure Identifier	Vector Identifier			
Channel TX			
Channel RX			
Global - General Purpose I/O (GPIO) Interrupts			
Global - Errors			
MGMT trap			

880

890

FIG. 8

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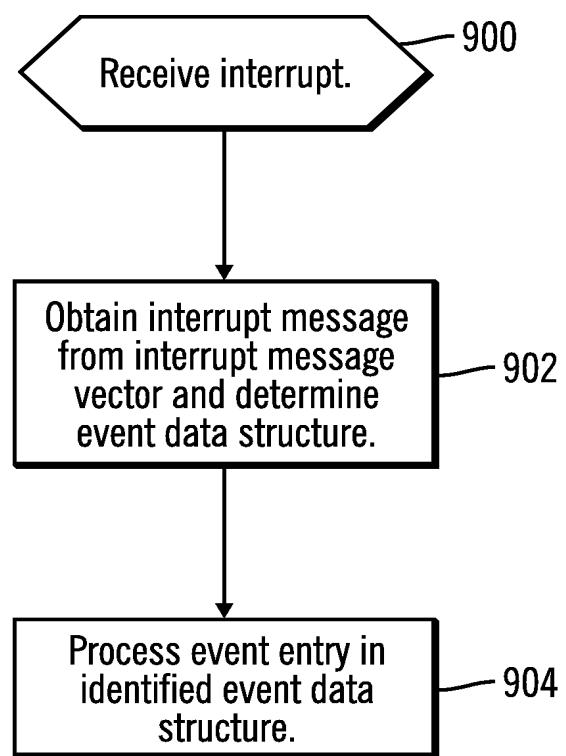


FIG. 9

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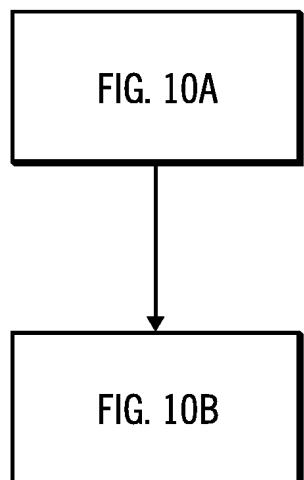


FIG. 10

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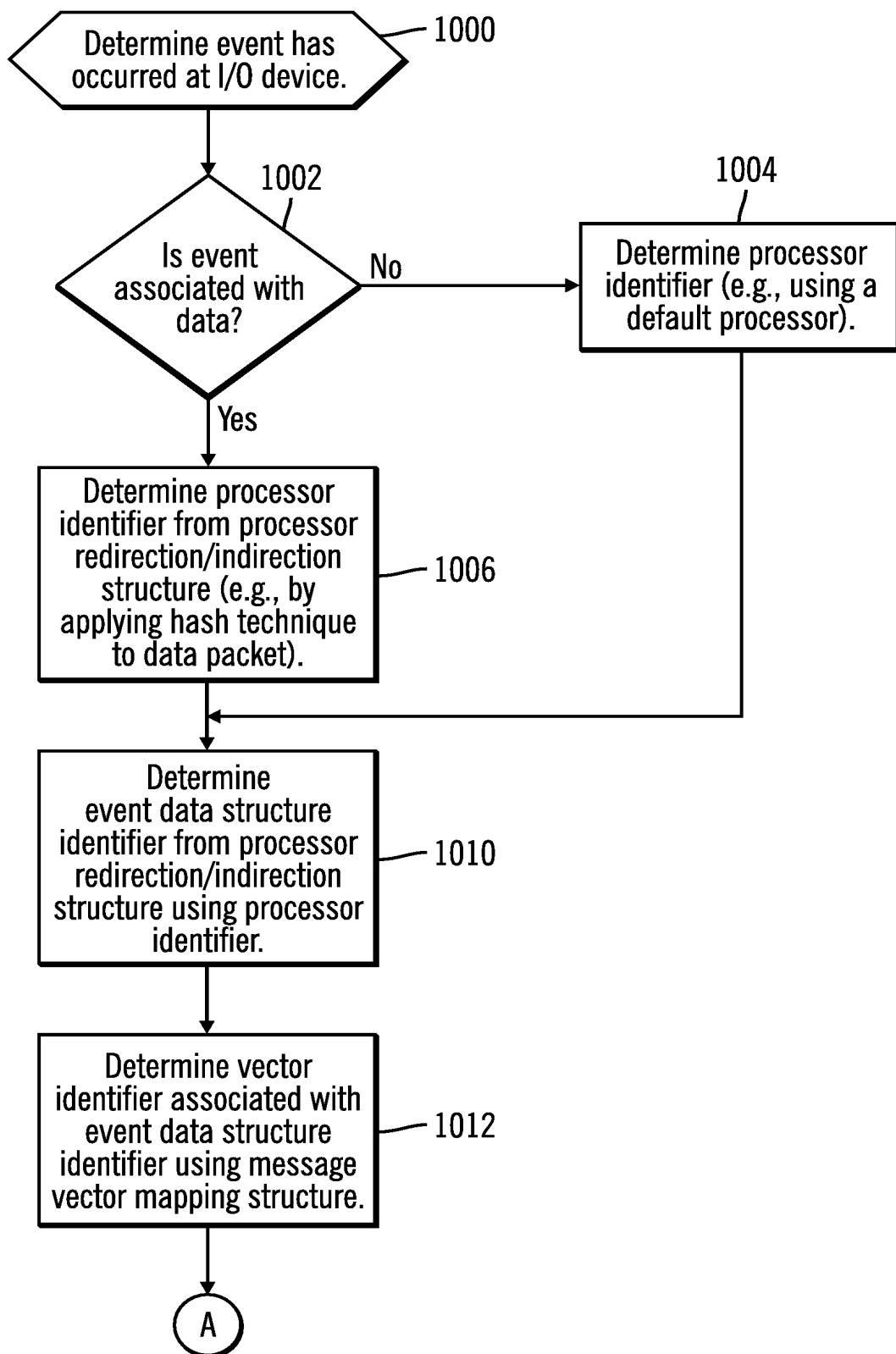


FIG. 10A

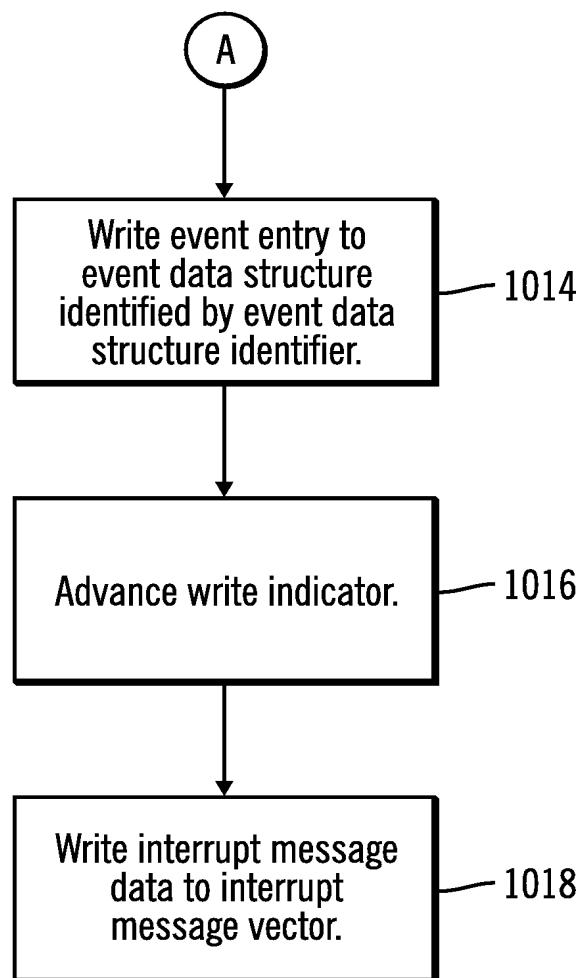


FIG. 10B



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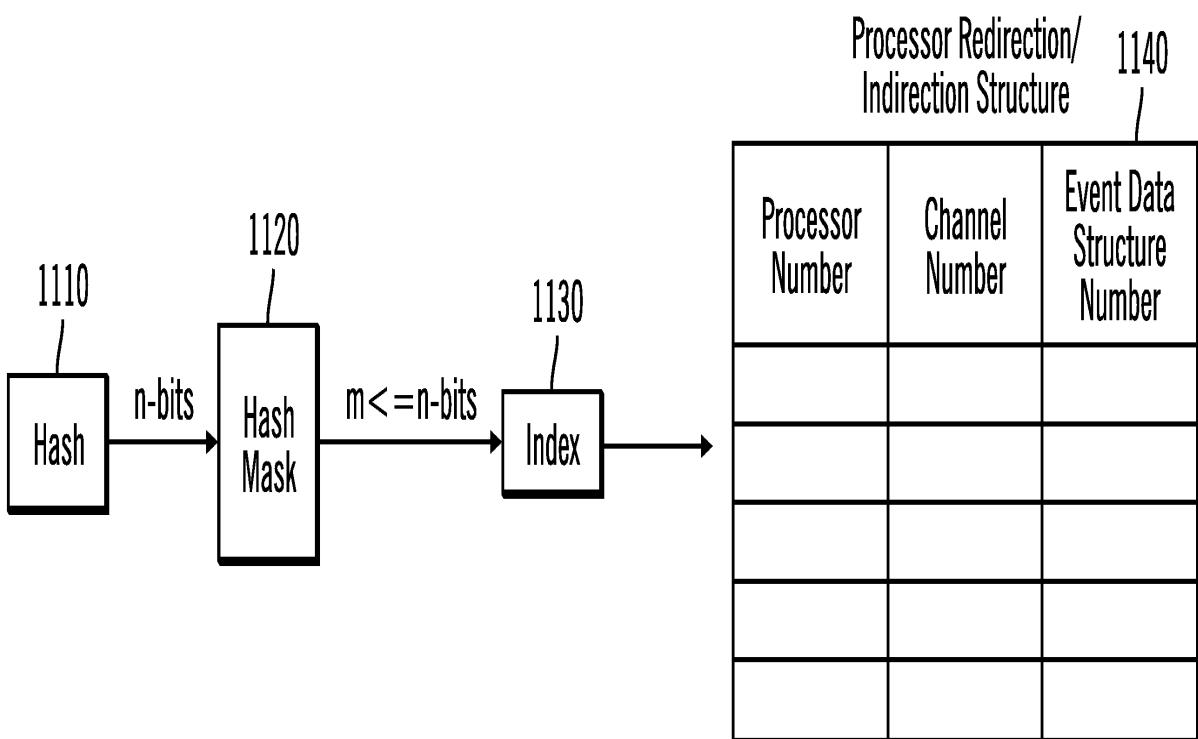


FIG. 11

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REPLACEMENT SHEET

INTERRUPT SCHEME FOR AN INPUT/OUTPUT DEVICE
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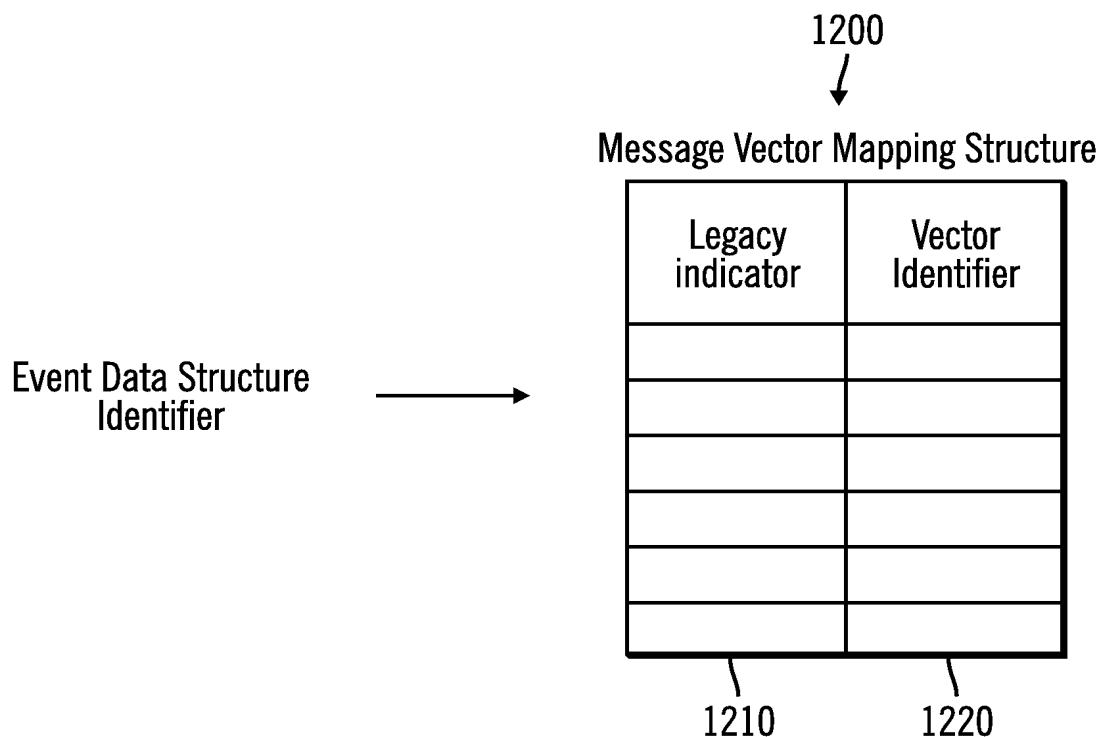


FIG. 12

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